MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.301 Solid State Circuits

Spring Term 2003 — Issued : April 25, 2003
Design Problem — Due : Friday, May 9, 2003

Work independently. Consultation with the 6.301 staff and other inanimate objects is encouraged. Computer and experimental verification of your final design is required. Read this handout thoroughly. Be sure to read anything written on the blackboard in the lab.

Introduction :

Operational amplifiers, characterized by high impedance differential inputs, low impedance single ended outputs, and very high gain, are extremely useful general-purpose bulding blocks for analog circuits. They can be used in any of a thousand applications. For this lab assignment, you are to design, build and test a simplified operational amplifier topology.

Project :

Using a conservative design approach, design an operational amplifier that meets the following specifications:

open-loop gain	$A \geq 20,000$
unity-gain frequency	$f_c \geq 100$ kHz
output swing	no spec
power supply voltages	± 15 V
transistors arrays[1]	CA3086/LM3086

These are minimal specifications. You should find it easy to design a circuit which exceeds some or all of these performance requirements. There are many acceptable solutions to this design problem. Feel free to use any topology you want (be sure that the first page of your lab report is a neatly drawn schematic with all parts clearly labeled). To help get you thinking, here is an example classic four transistor topology that can meet spec:

1. differential input based on a diff-pair
2. a common emitter gain stage
3. a emitter follower output stage

[1] We would like to limit you to one array (five transistors). However, since the substrate (pin 13) of the CA3086 must (absolutely, positively, MUST) be tied to -15V, you may not have enough flexibility to use all five transistors on one chip in your circuit. Thus, you may use either one or two chips to realize your five transistor circuit (be sure to remember that there is no matching of transistors on different chips). If you would like to explore a more complicated design with more transistors, you are cordially invited to discuss your ideas with the TA *first.*

Work out a preliminary design based upon typical numbers in the device spec sheets. Convince yourself that you understand this topology. Then go to lab use the curve tracer to measure β_0, r_o, and r_μ of your transistors. We ask that you measure the devices at several different operating points so that you can check for consistency in the data. Using these measurements, complete the design. Analyze the circuit by hand, making reasonable approximations.

Your design should be internally compensated for a unity-gain frequency of 100 kHz. In order to accomplish this, you will need to calculate the open-circuit time-constant resistance for you compensation capacitor (that will probably go around your second stage, like in the μA741).

Lab Work :

Construct your design and make all the required measurements: operating point, open-loop gain, unity-gain frequency, etc. Measure all of your component values. Make a plot of open-loop gain versus frequency for 1 Hz to 1MHz. Also, measure the step response rise-time and output slew-rate for closed loop topologies of gain 100, 10, and unity.

It is unlikely that your circuit will work uncompensated or open-loop. Thus you must calculate the correct compensation capacitor and include it the first time you build your circuit. Also, you do not have to run your op amp open-loop in order make the open-loop measurements. Instead, just divide the output amplitude by the (tiny) input amplitude at the input terminals in some closed loop topology.

Be sure to check your circuit thoroughly for oscillations with an analog scope before starting to take operating point measurements.