3.155J / 6.152J

MICROELECTRONICS PROCESSING TECHNOLOGY

TAKE-HOME QUIZ

FALL TERM 2003

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1) This is an open book, take-home quiz. You are not to consult with other class members or anyone else. You may discuss the solution to this exam only with the course staff.

2) **The quiz is due on Wednesday, November 12, AT THE START OF CLASS. Late exams will not be graded.**

3) There are parts of this quiz which will have more than one correct answer. Explain your answers, showing how and why you arrived at your solution either with analytical expressions, written explanations, or both.

4) Reference any source of specific material parameters, which includes title of article or book, journal, author and page number. For the class texts, you can simply indicate: Plummer, pg. #. You may find it faster and easier to use charts rather than equations, but in some situations that may not be possible and the theoretical equations (eg. Deal-Grove) must be used. Assume intrinsic diffusion.

5) Justify any assumptions (and you will certainly have to make some). Indicate where you make assumptions or approximations.

6) Some questions require qualitative answers. Keep them brief and focused on the most significant features.

7) GRADING: The submitted material should be clearly written and concise. The grader will spend a maximum of 30 minutes grading each submission. Poorly written, or overly voluminous reports will therefore be penalized.

PROBLEM STATEMENT

You have been hired (based on your performance in 3.155/6.152 and a strong desire to move to a warm climate) to develop the process flow for a new vertical power MOSFET that a company in Austin, Texas would like to market. You must design a process and figure out how to build it using their existing fabrication facility. Attached to this problem statement you will find:

i) A typical process flow sheet.
ii) A description of the microfabrication facility.
iii) A description of the vertical power MOSFET and the desired process specifications.

Part 1.

Develop a process flow for the fabrication of this device. Write your process description in the same form as the sample process flow attached, with supporting calculations appended. You need not worry about control wafers. Also included in the process flow should be rough cross-sectional drawings of the wafer at various steps in the process. In generating the process flow sheet, you will find that some steps will depend on future steps, and hence some iteration will be needed. Justification should be provided for all assumptions.

Part 2.

Draw the masks that would be needed to fabricate a device with the desired specifications. Include the bonding pads that will be used for packaging of the device. You should indicate the exact dimensions. What is the maximum number of devices/wafer?

Part 3.

Draw an exact cross-section of your device, with the masks generated in Part 2.

Part 4.

Without performing calculations, write a process flow which utilizes KOH etching rather than plasma etching to define the vertical MOSFET, and sketch the resulting device. Compare advantages and disadvantages of the two processes.

Notes regarding implants and diffusions:

1) Assume that the silicon dioxide / silicon interface is reflecting for the dopants (i.e. there is no diffusion across the boundary).
2) To simplify calculations, choose implant conditions such that the implant may be treated as an impulse of dopant at the surface for subsequent diffusions.
3) Assume all diffusions are intrinsic and non-interacting.
4) Intrinsic Diffusion Coefficients in Silicon (cm^2/s). Neglect diffusion at temperatures below 900°C. If you need a diffusion coefficient at another temperature, extrapolate using these numbers and assuming an exponential temperature behavior.

	900°C	1000°C	1100°C
Arsenic	2×10^{-16}	4×10^{-15}	5×10^{-14}
Boron	8×10^{-16}	2×10^{-14}	2×10^{-13}
Phosphorus	8×10^{-16}	1×10^{-14}	1×10^{-13}

TYPICAL PROCESS FLOW SHEET

Starting Material: 6" diameter, (100) silicon (n-type, 10^{14} cm^{-3}), 700 µm thick

Steps:

1) RCA clean
2) Grow SiO_2. Desired Thickness = 250 Å, Temp = 1000°C, Time = 20 minutes, Ambient = Dry 02. This oxide is to minimize channeling during the implant step.
3) Implant back-side of wafer to improve back-side contact. Energy = 100 keV , Dose = $5x10^{15}$ cm^{-2}, Element = Phosphorus.
4) Timed etch in BOE (Buffered Oxide Etch) to remove oxide. Rate = 1000 Å/min, Time = 35 seconds. (Includes 20 second over-etch to ensure completion.)
5) RCA clean
6) Grow SiO_2. Thickness = 1000Å, Temp = 950°C, Time = 20 minutes , Ambient = Wet O2 . This oxide is used to mask the implants in steps 9 and 12.
7) Photolithography - Mask #1. Dark Field
8) Timed etch in BOE (Buffered Oxide Etch) to pattern oxide. Rate = 1000 Å/min, Time = 80 seconds. End this process step with a photoresist strip.
9) Implant front-side of wafer with a n-type dopant. Energy = 50 keV, Dose = $2.6x10^{14}$ cm^{-2}, Element = Arsenic.
10) Photolithography - Mask #2. Dark Field
11) Timed etch in BOE (Buffered Oxide Etch) to pattern oxide. Rate = 1000 Å/min, Time = 80 seconds . End this process step with a photoresist strip.
12) Implant front-side of wafer with a p-type dopant. Energy = 20 keV , Dose = $5x10^{12}$ cm^{-2}, Element = Boron.
13) Timed etch in BOE (Buffered Oxide Etch) to remove all oxide. Rate = 1000 Å/min, Time = 80 seconds .
14) RCA clean
15) Grow SiO_2. Thickness = 1000 Å, Temp = 1100°C, Time = 40 minutes Ambient = Dry O2 . To facilitate hand calculations of the diffusion, we assume the Si/SiO_2 boundary is stationary when determining junction depths.
16) Dopant Drive-In. Temp = 1100°C, Time = 1.2 hours, Ambient = N2 .
17) Deposit LPCVD Polysilicon. The poly will be in-situ doped with Phosphorus. Thickness = 5000 Å Temp = 600°C. (We neglect diffusion during this deposition.)
18) Photolithography - Mask #3. Clear field.
19) Etch polysilicon in SF_6 plasma. (Assume infinite selectivity with oxide.) End this process step with a photoresist strip.
20) Strip polysilicon from back-side in SF_6 plasma.

MICROFABRICATION FACILITY

- 3000 ft^2 Class 100 cleanroom including 500 ft^2 Class 10 photolithography bay
- 18 gpm DI Water Plant (18MΩ-cm at point of use, teflon distribution system)
- N_2, Ar,and H_2, and O_2 gas plant with welded SS distribution system
- 1000 ft^2 testing and packaging area including automatic parametric tester, die-bond and wire-bonding machines, and a plastic injection molding machine.
- CAD system for process modelling and mask layout (masks are made at a local vendor using a tape generated from the CAD system)
- All equipment is designed for 6" silicon wafers, and a vendor of silicon wafers is available who can supply any dopant type, concentration, and orientation needed.

Process Equipment:

RCA Clean station

Acid Station

Solvent Station

8 furnaces:

1. Gate Oxidation (N_2, Dry 0_2)
2. General Purpose Oxidation (N_2, Dry and Wet 0_2)
3. Solid source boron doping
4. Solid source phosphorous doping
5. Dopant drive-in
6. Metal Sinter (400°C)
7. LPCVD Silicon Nitride (785°C, Growth Rate = 2000 Å/hour)
8. LPCVD Polysilicon (625°C, Growth Rate = 0.5µm/hour, in-situ doping capability)

Epitaxial Silicon available through a local vendor (1100°C, Growth Rate = 1000Å/min, n-type or p-type doping from 10^{14} cm^{-3} to 10^{19} cm^{-3})

Plasma Etcher (gases for Si, SiO_2, and Si_3N_4 etching)

Plasma Deposition System (for SiO_2 - 400°C)

Ion Implantation (available through a local vendor across the street)

Aluminum Sputter Deposition System

Full photolithography system:

Contact Aligner

min. feature size = 2 µm

alignment tolerance = ±2 µm

Photoresist Spinner, Develop Station, Ovens, and Plasma Stripper

Optical Microscopes, Ellipsometer, Dektak surface profiler, Sheet Resistivity Monitor

VERTICAL POWER MOSFET

Description:

A representative cross-section of this device is shown below. Specifications for the device are given below. The layout should be one which minimizes the total device size.

n+ Polysilicon Gate NMOS	Source Junction Depth = 1 µm
Channel Doping = 10^{16} cm^{-3}	Substrate Doping = 10^{20} cm^{-3}
Oxide Thickness = 1000 Å	Channel Length = 5 µm
W/L = 10,000	Bonding Pads = 200 µm x 200 µm
Polysilicon Thickness = 0.5 µm	Aluminum Thickness = 1 µm

Surface Concentration at Metal-Silicon Contacts > 10^{19} cm^{-3}

Cross-section (not to scale):